Fabrication and Integration of Nanostructures on Si Surfaces

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Introduction

Performance and integration density of large-scale-integrated circuits (LSIs) are growing exponentially with time, despite the limitations which were predicted more than 15 years ago. It is believed that this trend will remain unchanged for the coming decade. On the other hand, new nanofabrication techniques beyond conventional lithography are attracting increasing attention for the next generation of electronic devices. This is because optical lithography can never be used for the fabrication of structures of sizes smaller than a few nanometers. However, new device concepts using single electron charging and quantum effects are expected to be realized in this region. Although many nanofabrication processes have been proposed up to now, we have to consider whether any breakthroughs are likely using these techniques. One of the recent hot topics in nanofabrication is a technique using scanning probe microscopy (SPM).[1–4] This technique is very powerful in fabricating nanodevices for scientific studies as well as for the fabrication of guiding devices, which would come into practical use if nanolithography is established at the production level. However, the main drawback of this technique is the fact that it cannot be applied directly to the production of integrated devices. Because the main thrust of LSI technology is increasing integration density, the capability of wafer-scale processing is a crucial factor in nanofabrication.

To achieve wafer-scale control, self-organization techniques have recently been developed.[5–7] In this paper, we are using the word “self-organization”, which simply means that the nanostructures are formed naturally without lithographic techniques. One typical example is island formation, which takes place in the Stranski–Krastanow (S–K) growth mode in heteroepitaxy.[8–10] In the area of compound semiconductors such as InGaAs/GaAs, self-organized quantum dots have been intensively investigated to fabricate lasers with a low threshold current. In this application, size uniformity is the most important issue. In Si-based materials, the main applications are in the field of integrated devices. The arrangement of nanostructure positions on the wafer surface is equally important. Generally, self-assembling processes are thought to have the disadvantage of poor controllability. However, if controllability is dramatically improved, this concept becomes very attractive because nanostructures can be simultaneously fabricated on the whole wafer surface.

In this review, we describe our approach toward nano-integration.[5,7] We will show that the self-organization process can potentially produce uniform and artificially designed nanostructure patterns if we can control surface features such as surface reconstruction, atomic steps, and the phase boundaries of reconstructed domains. The first step of our strategy is surface structure control. A Si surface is one of the most perfect surfaces. Its structure can be controlled at the atomic level, as demonstrated in later sections. The second stage is fabrication of semiconductor hetero-nanostructures whose formation sites are determined in advance by surface structure controls. Here, we demonstrate that formation of a Ge quantum dot network can be achieved using this approach. Electronic devices require insulating layers and conducting layers in addition to the semiconductor nanostructures. The third stage of our approach is the fabrication of semiconductor/insulator/conductor nanostructures from well-controllable semiconductor structures. For this target, reaction selectivities in heterostructures are utilized. Some of the techniques shown here cannot be applied directly to nano-integration, but our basic idea is the compatibility of atomically controlled nanofabrication and wafer-scale

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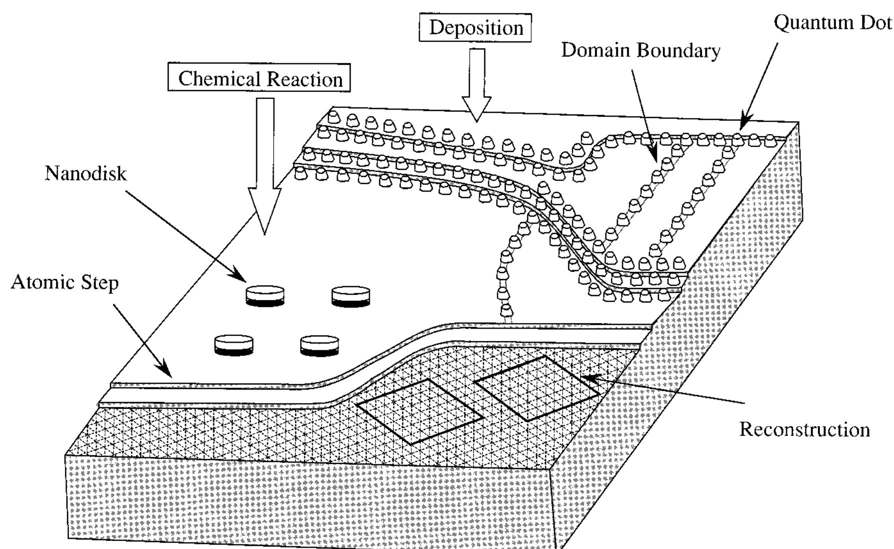

FIGURE 1. Key idea of nanofabrication based on surface structure control. Nanowires and quantum dots are self-organized on Si surfaces by controlling reconstruction, atomic steps, and reconstructed domain boundaries as nanofabrication templates.

integration. Throughout this account, we mainly discuss the results from Si(111) surfaces. In current Si-MOS (metal oxide semiconductor) technology, the (001) surface is exclusively used because its Si/SiO_2 interface exhibits lower density of states compared with other surfaces. However, if we try to control self-organizing nanostructures, the (111) surface has the advantage that an atomically flat surface and a well-defined step/terrace structure can be easily obtained even by chemical treatment.[11,12]

Nanofabrication Based on Surface Structure Control

Atomic features on clean Si surfaces are classified into three categories: surface reconstruction, out-of-phase boundaries (OPBs) formed between reconstructed domains, and atomic steps. Figure 1 shows nanofabrication guided by the surface structures.

On a Si(111) surface, the 7 × 7 reconstruction which is explained by the DAS (dimer, adatom, and stacking fault) structure[13] is the stable phase at room temperature. Because a unit cell of the 7 × 7 reconstruction is large, this could be a template for nanofabrication. The unit cell has two subunits: a faulted half with a stacking fault (SF) at the second layer and an unfaulted half without an SF.[13] These subunits exhibit different reactivities for adsorption.[14,15] This feature might be applicable to nanofabrication. These subunits, however, are triangles with 2.7 nm sides, too small to expect practical semiconducting properties. A more promising application of 7 × 7 unit cells is achieved by combining a couple of unit cells to form two-dimensional islands or wires. In this technique, the structure size is quantized by the 7 × 7 unit cell and therefore the fluctuation in size of the resulting nanostructures is minimized. One example is a 7 × 7 nanowire formed on a Ga-adsorbed Si(111) surface.[16] The 7 × 7 reconstructed wirelike region, 7 nm in width, was formed along an atomic step and the nucleation was controlled by scanning tunneling microscopy (STM). Figure 2 shows

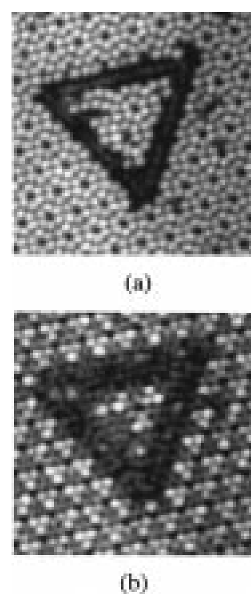

FIGURE 2. STM images of nanostructures fabricated by solid-phase epitaxy of a thin Ge film deposited on a Si(111) surface: (a) a positive sample bias and (b) a negative sample bias. The image size is 17 × 17 nm^2. The triangular region is twinned with respect to bulk, and its size is determined by the surface reconstruction, which was initially 7 × 7 and became a 5 × 5 structure during the solid-phase epitaxy.

another example of nanostructures in which the size is controlled through the surface reconstruction phenomenon.[17] In this process, an amorphous Ge layer 4 ML (monolayers) thick was deposited on a clean Si(111) surface. At this stage, the framework of the 7 × 7 reconstruction at the interface was preserved.[18] The sample was then annealed under ultrahigh vacuum (UHV) around 400 °C. As the Ge layer was epitaxially crystallized, faulted triangles with longer sides, typically 14 times the (111) unit cell, appeared. This structure was formed from one unfaulted half and three faulted halves. Together, they form a region which is twinned with respect to the substrate. With annealing up to 640 °C, the number of

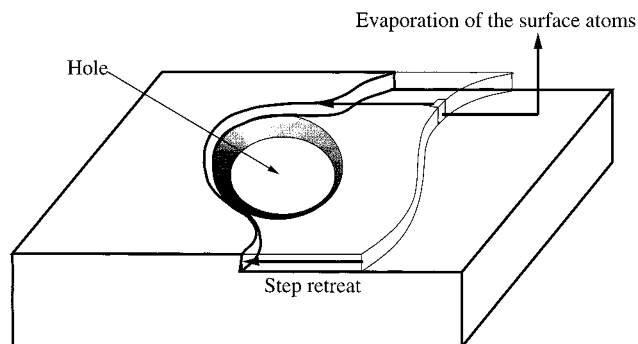

FIGURE 3. Key idea of step rearrangement control by using an etched pattern. The step motion induced by adatom evaporation during heating is pinned at the pattern periphery. After the pattern disappears, a step bunch remains around the hole position.

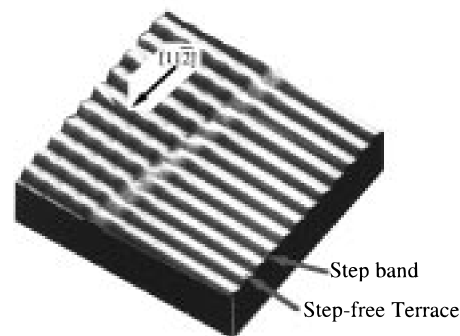

FIGURE 4. AFM image of step bunches formed on a Si(111) surface by using the process shown in Figure 3. The Si substrate is misoriented toward the ⟨11−2⟩ direction by 1.5° from the exact (111) surface. The patterns used to control the step arrangement were hole arrays with a pitch of 3.5 μm (right region) and 4.0 μm (left region). The step bunches are branched or combined at the boundary between the two regions because of the different hole pitches.

the twinned regions decreases but their size increases. Finally the triangle shown in Figure 2 remains on the 5 × 5 reconstructed surface, which is the stable reconstruction on thin Ge layers commensurately grown on Si(111) surfaces. The technique of fabricating nanostructures by using reconstruction as a quantization unit has the advantage that size fluctuation is suppressed. However, the control of nucleation sites is difficult unless we use another method to control them.

The 7 × 7 reconstruction is the only template if the surface is perfect. However, there are always two kinds of imperfection on the surface: atomic steps, which originate in the misorientation of the substrate, and OPBs, which are generated by the coalescence of independently nucleated 7 × 7 domains. These are disordered regions, but also nucleation sites from the point of nanofabrication. The 7 × 7 nanowire on a Ga-adsorbed surface described earlier is one example where the wire is formed along a step. Another example of nanostructures forming on steps are quantum dots whose nucleation takes place preferentially on the steps as shown in Figure 1. It is known that phase boundaries are also preferential nucleation sites. In general, steps and phase boundaries are randomly distributed and, therefore, the nanostructures guided by these disordered regions exhibit no ordering. However, if we can control the position of the nucleation, regularly arranged nanostructures can be obtained. In particular, step arrangement control plays a crucial role because steps exist on any surface and can be nucleation sites for subsequent crystal growth and initiation sites in chemical reactions.

Local step arrangement on the Si(111) surfaces is determined by the substrate misorientation direction and the misorientation angle.[19−22] When the surface is misoriented toward ⟨−1−12⟩, steps are distributed uniformly without step bunches. On the other hand, a surface misoriented toward the ⟨11−2⟩ direction is separated into step-bunched regions and wide 7 × 7 terraces. This can be utilized to form locally ordered step arrangements.[23,24] However, wafer scale control requires another approach. To arrange steps regularly on Si(111) surfaces, we have developed a technique using etched patterns formed by the lithographic method.[23,24] When the Si surface is heated at high temperatures in UHV, the adatoms (atoms weakly bound to the surface) evaporate from the terrace and, as a result, its density decreases. Because adatoms are supplied from step edges, step retreat takes place. If a small hole is formed as shown in Figure 3, the step motion is pinned at its periphery because the sidewall of the hole is a bunch of steps; moving steps are combined with the steps forming the sidewall. On further heating, more steps are pinned at the periphery to form a step bunch, and the hole becomes shallower due to the step retreat and the adatom inflow. Finally, the hole disappears and regularly ordered step bunches are formed. When the holes are arranged to make a particular pattern, the resulting step bunches are also arranged according to the hole pattern. Figure 4 is an atomic force microscopy (AFM) image of a step-controlled surface. In this demonstration, a Si(111) wafer misoriented toward the ⟨11−2⟩ direction by 1.5° was used and the pattern was fabricated by the standard Si process, including optical lithography and reactive ion etching. In the early stage of heating at 1300 °C the holes were trimmed, resulting in a conical shape, and bottom planes oriented exactly to the (111) surface appeared. After the wafer was heated for a couple of minutes at 1300 °C, the hole pattern disappeared and the step bunches formed along the periphery of the holes. A closer examination of the step network shown in Figure 4 suggests that the region on the right consists of only wide step bunches, whereas the region on the left includes crossing step bunches. The step network on this surface is schematically shown in Figure 5. The difference between the two regions is partially due to the difference in the hole size; larger holes were filled later than the small holes. Another reason is the difference in the boundary conditions as shown in Figure 5. The crossing steps, generated by the misalignment of the hole pattern and the misorientation direction, move from the left to the right. At the right side (not seen in Figure 4), a trench is formed and the crossing steps are absorbed into the trench edge. The pitches of the left and the right regions are different, and step bunches are branched out at the boundary. Therefore, the crossing steps do not easily move across the

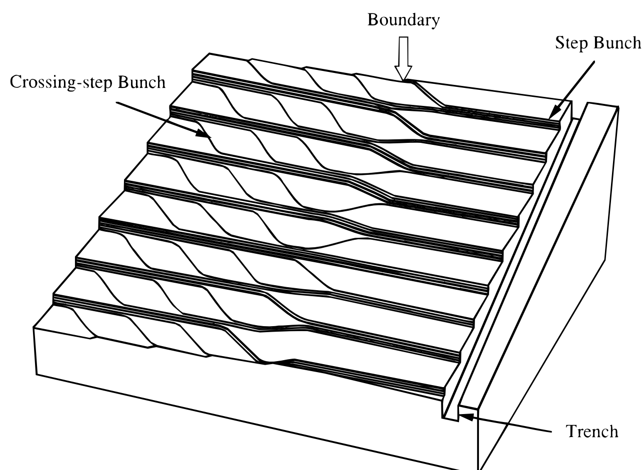

FIGURE 5. Schematic of the step network formed as shown in Figure 4. The step network in the left region consists of main step bunches and branch bunches crossing the terraces, whereas that in the right region exhibits only main bunches. This difference is due to the boundary conditions.

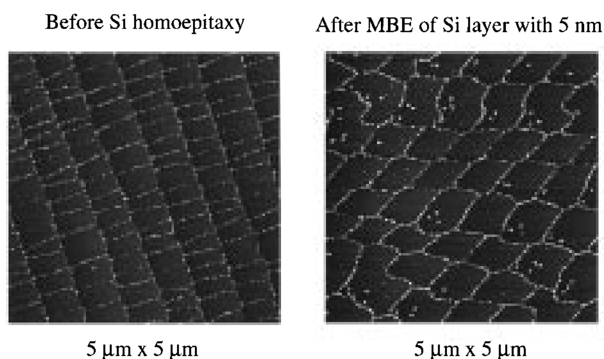

FIGURE 6. Evolution of the step-OPB network during the step-flow growth on Si(111). The initial surface (a, left) was prepared by buffer layer growth followed by annealing at 900 °C. After 1 nm growth at 750 °C, the network (b, right) was formed. After the network formation, small Ge islands were grown on the steps and OPBs.

boundary. These results clearly demonstrate that the step arrangement is controllable on a large scale. In other words, step networks designed to form a specific circuit can be formed. The minimum pitch of the step bunches is determined by the resolution of the lithography used, but nanostructures which nucleate at steps are arranged according to the step network. Therefore, the step network shown here can be used as a template for nanointegration.

Control of the phase boundaries (OPB) is less general in comparison with step control but equally important for the Ge quantum dot network on Si(111) surfaces. The OPBs are generated when the (111) surface is cooled from high temperatures via the "1×1" to 7×7 phase transition temperature. At this stage, nucleation of 7×7 domains is random. After the completion of the phase transition, the OPBs cross the terraces perpendicularly to the steps as shown in Figure 6a,[25] but their positions are random. We used step-flow growth to regulate the number of OPBs.[25] When Si atoms are deposited on the surface, on which steps and OPBs coexist, Si atoms are incorporated preferentially at the cross-points of the steps and the OPBs. Therefore, the step flow speed is faster around the cross-points than around the other regions. This makes the step shape wavy and two close OPBs tend to approach each other, resulting in coalescence. Figure 6 shows an evolution of the step-OPB network. Here the network was decorated by small Ge islands after the step-OPB network formation. The Ge island growth on the network will be described later.

Another application of step flow growth is the step arrangement control on a patterned surface. In this case, the step-flow speed in a particular pattern is regulated by its boundary conditions and we can obtain unique step arrangements.[26] Step arrangement on periodically patterned Si(001) surfaces has also been reported.[27]

Nanofabrication Based on Heteroepitaxy

In compound semiconductors, a variety of novel properties were found by using heteroepitaxial layered structures and have been applied to electronic and optical devices. Si exhibits excellent properties such as high thermal stability, extremely low dislocation density, and availability of thermal oxide films for surface passivation. However, Si has the disadvantage of material incompatibility for forming heterostructures; Ge and SiGe alloy are the only practical candidates. Therefore, the control of Ge growth on Si surfaces is an important issue in Si technology. The lattice constant of Ge is larger than Si by 4%, and the critical thickness for commensurate growth is about 4 ML. Before 1990, layer-by-layer growth with low dislocation density was the main target. To achieve this, novel growth techniques such as using surfactants were developed.[28] In 1990, the growth mode of coherent Ge islands was found[29] and the common interests moved to three-dimensional nanofabrication. On Si(001) surfaces, bimodal coherent island growth has been established, though its mechanism is still being debated.[30–32] When the Ge coverage is low, pyramidal islands[30] are grown. As the coverage increases, larger islands called "domes" with many facets become predominant.[31,32] These quantum dots are now hot topics from the point of view of device applications as well as from a basic scientific point of view,[33] because these islands are dislocation-free and the growth mode is new. Here, we focus on Ge growth on other Si surfaces from the point of nanofabrication: Si(111) and Si(113).

On Si(111) surfaces, coherent island growth is not a commonly observed mode. However, we can apply the surface structure controls mentioned in the last section to achieve formation of an island pattern. The Ge quantum dot networks shown in Figure 6 are typical examples formed on Si(111) surfaces. These were fabricated as follows.[34,35] First, an amorphous Ge layer, 1 nm thick, was deposited on step-controlled Si(111) surfaces and then annealed. During annealing, excess Ge beyond the critical coverage formed islands. Here, the framework of the 7×7 reconstruction is preserved before the nucleation of the islands, and consequently, OPBs are also preserved at the interface between the Ge layer and the Si surface. Since

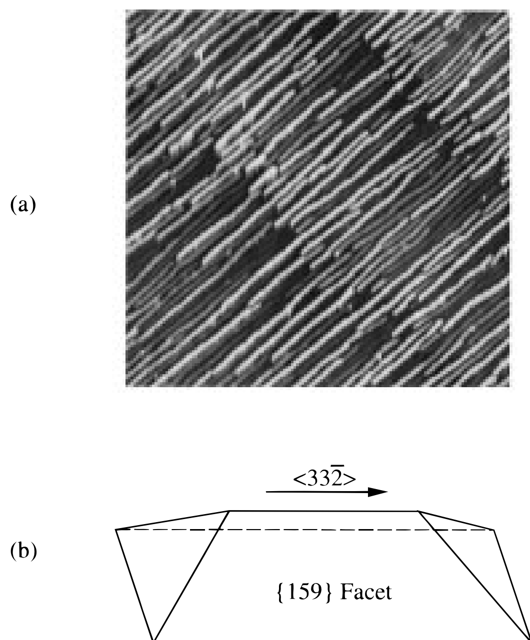

FIGURE 7. (a) AFM image of Ge wirelike islands grown by depositing 6.4 ML Ge at 400 °C on a Si(113) surface. (b) Schematic of the wirelike island. The elongated facets are {159}.

the nucleation of Ge takes place preferentially on the steps and OPBs, the Ge islands are arranged according to the step-OPB network. The average size of the Ge islands can be controlled by the coverage of deposited Ge and the annealing temperature, but island uniformity remains uncontrolled.

The Si(113) surface is one of the stable high-index surfaces. Because this surface is anisotropic in elastic properties, it is a suitable candidate to examine the possibility of shape and size controls of Ge islands. Figure 7a shows an AFM image of Ge islands grown on a Si(113) surface by molecular beam epitaxy (MBE).[36] The coverage of Ge was 6.4 ML, and the substrate temperature was 400 °C. The Ge islands are wirelike and elongated toward ⟨33−2⟩. The size was less than 2 nm in height, from 10 to 32 nm in width, and from 10 to 600 nm in length. Transmission electron microscopy (TEM) images showed that these islands are coherent. The Ge coverage and the growth temperature for the coherent island growth are between 5 and 8 ML and 400 and 500 °C, respectively. Note that the islands are elongated perpendicular to the steps; a wirelike shape was not formed by nucleation along the steps. From the RHEED (reflection high-energy electron diffraction) observation, it was found that the islands are {159}-faceted as shown in Figure 7b. The wirelike shape is explained by the surface stress anisotropy. Interestingly, some islands grow continuously across steps. This suggests that surface stress relaxation propagates across steps via the subsurface region and induces nucleation on the adjacent terrace. The result indicates that island shape can be controlled by employing an appropriate anisotropic surface. The (113) surface is not a commonly used surface, but (113)-facet regions can be formed on (111) or (001) substrates by using etched patterns. If we could give anisotropic surface stress to Si(111) or (001) surfaces, shape control would be possible.

The size uniformity of the islands grown by the S−K growth mode is generally insufficient for device applications. Kamins et al. have shown that uniform Ge islands are positioned along the edges of a mesa pattern.[37] Another approach to controlling size distribution was proposed by Tersoff and Lagally.[38,39] This control is based on the formation of Si/Ge multilayers. The Ge layers consist of a wetting layer and coherent islands, and consequently, their surfaces are not flat. Because the Ge islands are coherent, the Si spacer layer is also grown without dislocation formation. After the Si spacer layer grows, its surface recovers flatness, but the surface potential for the next Ge growth is modulated by the embedded Ge islands. When Ge islands are grown again on the Si spacer layer, Ge nucleation takes place preferentially above embedded Ge island sites, resulting in the vertical alignment of the Ge islands. At this stage, uniformity in island density and size is improved. This is explained by a band-pass filtering effect for nucleation sites. When two embedded Ge islands are closely placed, the potential formed by these islands on the Si spacer surface is smoothed to form one potential minimum. In more general terms, the island density decreases just above the region of high-density embedded Ge islands. Above a region of low density of Ge islands, on the other hand, new nucleation sites appear, resulting in an increase in the island density. We employed this technique to control the size and shape distribution of Ge islands on Si(113).[40] Figure 8 shows (a) an AFM image of the top surface and (b) a cross-sectional TEM image of a Ge/Si multilayer on Si(113). The individual deposition coverages of the Ge layer and the Si spacer layer are 6.4 and 30 ML, respectively, and 10 Ge layers and 9 Si spacer layers were stacked at 400 °C for the sample shown in Figure 8a. The islands observed on the 10th Ge layer shown in Figure 8a are also wirelike and {159}-faceted. The nucleation sites are clearly aligned vertically above the embedded Ge island, as seen in Figure 8b. The average island size becomes larger on the top Ge layer compared with that on the first Ge layer shown in Figure 7, and the size fluctuation becomes smaller. Under the present growth conditions, the island shape was always elongated. When the substrate temperature was 450 °C, the island shape on the first Ge layer became wider and shorter. After multilayer formation, the wirelike islands changed to "dash"-like ones, 3 nm wide, 4 nm high, and 70 nm long. These results show that island shape is controlled by the growth conditions of the multilayered structure as well as size distribution.

Nanofabrication Based on Surface Reactions

The third stage of the present strategy is semiconductor/insulator/conductor nanofabrication based on chemical reactions. In Si−Ge systems, chemical bonds of Si with different atoms are generally stronger than those of Ge. This reaction selectivity is effectively utilized for nano-

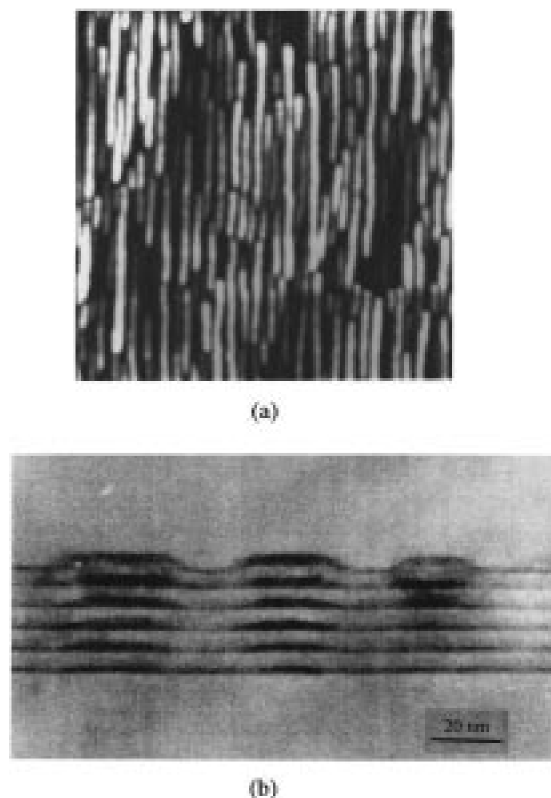

FIGURE 8. Control of Ge island growth by the formation of a multilayer of Ge-island layers and Si-spacer layers: (a) AFM image of Ge islands grown on the top surface of 10 bilayers of Si/Ge grown on the Si(113) surface; (b) cross-sectional TEM image of a Ge/Si multilayered structure in the ⟨33−2⟩ injection. This shows the vertical alignment of the Ge islands.

fabrication. The most important chemical reaction in Si technology is oxidation to form high-quality SiO_2 layers. When a SiGe alloy layer is thermally oxidized, selective oxidation of Si takes place and Ge is segregated from the formed SiO_2 overlayer, forming an accumulation layer at the SiGe/SiO_2 interface.[41] In the case of oxidation of a thin Ge layer on Si surfaces, GeO forms on the Ge surface below 250 °C. Upon annealing, oxygen changes its bonding partner from Ge to Si.[42,43] This is not directly applied to nanofabrication, but reaction selectivity can be used to incorporate insulating layers in semiconductor nanostructures. Here we show the oxidation process of a Si/Ge multilayer to demonstrate that the bonding partner exchange reaction (Ge−O + Si → Si−O + Ge) can be used to self-assemble semiconductor/insulator multilayers.[44] Figure 9a shows the experimental procedure. The sample was a Si/Ge five-level multilayer, and oxygen ions were implanted into it at room temperature. Then the sample was annealed at 600 °C. Figure 9b shows the depth profile of Si, Ge, and O analyzed by Auger electron spectroscopy (AES). In ion implantation with a single energy, distribution of the implanted ions generally follows a Gaussian shape. The oxygen profile in Figure 9b, however, exhibits three peaks at the Si/Ge interfaces and at the thin Si interlayer. In the Si/Ge system, oxygen forms a bond preferentially with Si. Therefore, if the oxygen implanted into the Ge layers is mobile, oxygen moves to the Si/Ge

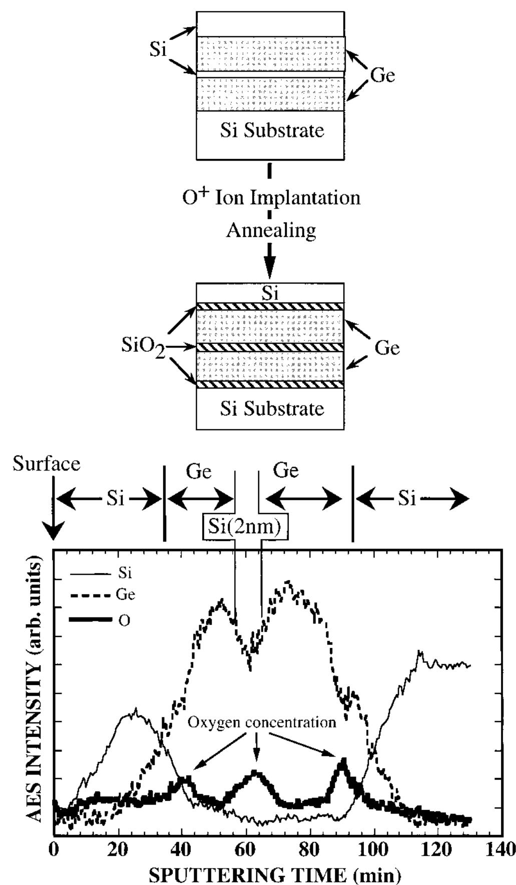

FIGURE 9. Selective oxidation of interfaces and a very thin Si interlayer in Si/Ge multilayers. An amorphous Si (30 nm)/Ge (14 nm)/Si (2 nm)/Ge (14 nm)/Si (30 nm) five-level layer was deposited on a Si surface. Oxygen ions of 30 keV were implanted, and the sample was annealed at 600 °C. The dose of oxygen implantation was 1×10^{17} cm^{-2}. The depth profiles taken by AES exhibits clear oxygen concentration at the Si/Ge interfaces and at the 2 nm Si interlayer. The difference between Auger electron energy from elemental Si and that from oxidized Si is large. In this plot, the Auger signal from elemental Si is plotted, and therefore there are no peaks from the SiO_2 layers.

interfaces and forms SiO_2. In this experiment, the substrate temperature during implantation was kept below 100 °C. Nevertheless, a concentration of oxygen was observed at the Si/Ge interfaces and the Si interlayer just after the implantation. This suggests that implanted oxygen atoms are moved by the subsequent implantation until they reach the interfaces. We believe that oxide layer formation in Si/Ge nanostructures is basically possible by applying this interface oxidation process.

The final elements required for device fabrication are conducting layers. Control of semiconductor/metal structures on an atomic scale is generally difficult due to differences in crystal structures, alloying at semiconductor/metal interfaces, poor adhesion, and so on. However, the silicides of some metals grow epitaxially on Si surfaces and form an abrupt interface. In particular, $CoSi_2$ has the advantage of small lattice mismatch with Si (1.2%) and atomic level control of its interface is possible. Reaction selectivity of Co with Si and Ge was demonstrated in the in-diffusion onset temperatures of thin Co films deposited

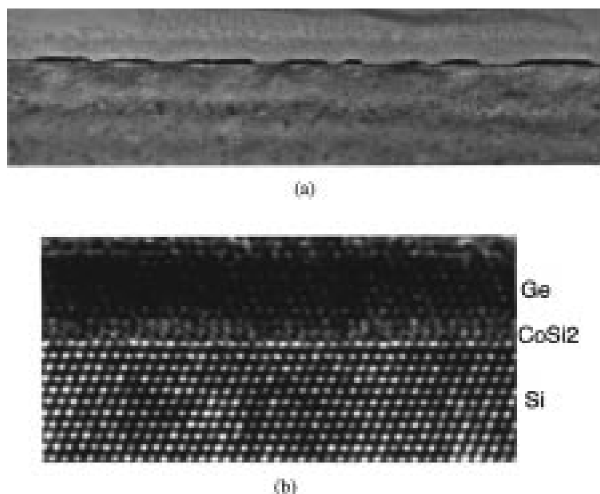

FIGURE 10. Cross-sectional TEM images of Ge/$CoSi_2$/Si nanodisks fabricated from a Co/Ge/Si layered structure: (a) wide view; (b) lattice image. The Ge and $CoSi_2$ layers were epitaxial in native.

on Si and Ge surfaces. Co on a Ge surface begins to diffuse inward upon annealing at about 150 °C, whereas Co on a Si surface does not diffuse below 300 °C.[45] This diffusion selectivity suggests the possibility of interface silicidation in Ge/Si structures. In our experiments, 3 ML Ge was first deposited on a Si(111) surface at room temperature and then a Co overlayer was formed on it. After the sample was annealed at 460 °C, nanodisks typically 10 nm in diameter were formed, as seen in the cross-sectional TEM image of Figure 10a.[46] The layer structure of the nanodisks was investigated by using medium-energy ion scattering (MEIS) and a lattice image TEM, as shown in Figure 10b.[46] It was found that the nanodisks consist of an epitaxially grown Ge top layer and a $CoSi_2$ interlayer. Although the formation process of the nanodisks has not been clarified, the results show the possibility of a novel nanofabrication technique based on a reaction-induced structural change.

Summary

In this account, we have described nanofabrication techniques on Si surfaces according to a strategy developed in our laboratory: that is, integration of atomically controlled nanostructures on a wafer scale. The approach consists of three steps: (1) control of surface structures such as atomic steps and phase boundaries of reconstructed domains to form a template of nanofabrication, (2) control of self-organization processes to fabricate semiconductor nanostructures, and (3) control of chemical reactions to form semiconductor/insulator/conductor nanostructures which are required for device applications.

To understand the mechanisms of nanofabrication presented here, basic research on surface physics and chemistry is required. At the same time, we have to consider how this approach will bring about a breakthrough in semiconductor technology. The current MOS devices will undoubtedly continue to be the leading device in information processing systems. However, information processing is increasingly expanding its application in social issues. This implies that binary logic as the basis of MOS technology will not always be the best architecture. To handle information in human life, different processing systems, and consequently a novel device concept, will be required.[47,48] We believe that our approach is one of the candidates for working toward realizing future Si technology.

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